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10/567,241	01/04/2007	Takuji Maeda	0074/065001	9459

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Randolph A Smith
Smith Patent Office
1901 Pennsylvania Ave NW
Suite 901
Washington, DC 20006

EXAMINER	
BERTRAM, RYAN	
ART UNIT	PAPER NUMBER
2187	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/567,241	MAEDA ET AL.	
	Examiner	Art Unit	
	RYAN BERTRAM	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,14-16 and 22* is/are rejected.

7)☒ Claim(s) *10-13,17-21 and 23-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The examiner acknowledges the applicant's submission of the amendment dated 3/16/2010. At this point claims no have been amended and claims 1-27 are pending in the instant application.

I. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9, 14-16 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Hayashi et al. (US 5,434,618).

1. Regarding claim 1, Hayashi discloses a semiconductor memory card which is used in connecting to an access device, comprising:

a host interface which transmits a control signal and data to the access device and receives a signal from the access device **[see Fig. 2, element 31, interface]**;

a nonvolatile memory in which a plurality of continuous sectors are grouped into an erase block as a minimum unit for data erasing **[see Fig. 2. element 34 & Col. 1, lines 25-44; non-volatile EEPROM with collective erasure ability]** and which

includes an address management information area and user data area **[see Col. 5, lines 56-67 and Col. 6, lines 1-3; memory stores data memory allocation table]**;

a memory controller which controls erasing, writing and reading of data for said nonvolatile memory **[see Fig. 4, element 16 & Col. 5, lines 22-30; memory controller controls access to memory]**;

a memory for card information storage including a card information storage part which stores information on access condition as condition at least at the time when said access device accesses said semiconductor memory card and access performance which said semiconductor memory card realizes when said access device performs access on said access condition **[see Col. 5, lines 22-67; memory area contains card attribute information containing information regarding the kind, speed, and state of the memory]**, and

a control part which controls each part on the basis of the control signal acquired via said interface **[see Col. 5, lines 22-30; memory controller controls access to memory]**.

2. Regarding claim 2, Hayashi discloses the semiconductor memory card according to claim 1, wherein said card information storage part stores

first information on physical characteristics of in said semiconductor memory card **[see Col. 5, lines 40-45; kind of memory card is stored]**, and at least one of

second information on access condition **[see Col. 5, lines 58-65; used and unused location information]**

third information on said access rate of said semiconductor memory card as information on said access performance **[see Col. 5, lines 45-50; storing speed]**, and

fourth information on abnormal process of said semiconductor memory card.

3. Regarding claim 3, Hayashi discloses the semiconductor memory card according to claim 2, wherein the third information in said card information storage part includes a flag representing rate performance of said semiconductor memory card as said information on access rate **[see Col. 5, lines 40-55; memory card speed stored in a register (flag)]**.

4. Regarding claim 4, Hayashi discloses the semiconductor memory card according to claim 1, wherein said card information storage part stores at least first information on physical characteristics in said semiconductor memory card **[see Col. 5, lines 40-45; kind of memory card is stored]**, second information on said access condition **[see Col. 5, lines Col. 5, lines 58-65; used and unused location information]**, and third information on access rate of said semiconductor memory card as information on said access performance **[see Col. 5, lines 40-55; access rate]**.

5. Regarding claim 5, Hayashi discloses the semiconductor memory card according to claim 4, wherein said control part, in response to a request from said access device, reads information on access condition for accessing said semiconductor memory card, and information on access rate when accessing to said semiconductor memory card on

said access condition from said card information storage part, and transmits the information to said access device **[see Col. 6, lines 33-40; attributes and access rate read from card by access device]**.

6. Regarding claim 6, Hayashi discloses the semiconductor memory card according to claim 4, wherein said control part, in response to information on access condition designated by said access device, reads information on access rate when accessing the semiconductor memory card on said access condition from said card information storage part, and transmits the information to said access device **[see Col. 6, lines 33-40; attributes and access rate read from card by access device]**.

7. Regarding claim 7, Hayashi discloses the semiconductor memory card according to claim 4, wherein said control part, in response to information on access rate designated by said access device, reads information on access condition to said semiconductor memory card required to meet said access rate from said card information storage part, and transmits the information to said access device **[see Col. 6, lines 33-40; attributes and access rate read from card by access device]**.

8. Regarding claim 8, Hayashi discloses the semiconductor memory card according to claim 4, wherein said control part, when reading information on access condition designated by said access device and information on access rate from said card information storage part and accessing said semiconductor memory card on said

access condition, determines whether or not the access rate is met and transmits a determination result to said access device **[see Col. 6, lines 33-40; access rate read from card by access device and card utilizes rate information]**.

9. Regarding claim 9, Hayashi discloses the semiconductor memory card according to claim 4, wherein the third information in said card information storage part includes a flag representing rate performance of said semiconductor memory card as said information on access rate **[see Col. 5, lines 30-60; access rate information stored in register in memory]**.

10. Regarding claim 14, Hayashi discloses the semiconductor memory card according to claim 1, wherein said card information storage part has an access performance basic information list which holds various process time and process unit size in said semiconductor memory card according to an access method, and in response to a request from said access device, said control part transmits said access performance basic information list to said access device **[see paragraph 87; number of bytes per sector]**.

11. Regarding claim 15, Hayashi discloses the semiconductor memory card according to claim 1, wherein said card information storage part holds process unit size of said semiconductor memory card, access method and access rate in the case where access condition containing process contents are changed, and in response to request

of said access device, said control part transmits information on said access rate to said access device **[see Hayashi Col. 6, lines 33-40; attributes and access rate read from card by access device]**.

12. Regarding claim 16, Hayashi discloses an access device for accessing a semiconductor memory card in which a plurality of continuous sectors are grouped into a block as a minimum unit for data erasing and stored data is managed according to a file system comprising:

a card information acquisition part for acquiring information on access condition as condition at the time when said access device accesses said semiconductor memory card and access performance which said semiconductor memory card realizes when said access device performs access on said access condition from said semiconductor memory card **[see Col. 6, lines 25-40; when the memory is connected to the access device, the access device acquires the memory card attributes, thus necessitating a card acquisition part in the access device]**;

a card use condition storage part for storing information on access condition which can be used when said access device accesses said semiconductor memory card and information on access rate desirable for said semiconductor memory card **[see Col. 6, lines 25-40; when the memory is connected to the access device, the access device acquires and analyzes the memory card attributes, thus necessitating a card use condition storage part in the access device in order to store and analyze the received memory card attributes]**;

an access condition determination part for determining access condition on the basis of the information acquired by said card information acquisition part, information on access performance of said semiconductor memory card and information stored in said card use condition storage part **[see Col. 6, lines 25-40; when the memory is connected to the access device, the access device acquires and analyzes the memory card attributes, thus necessitating an access condition determination part in the access device in order to interpret the received memory card attributes]**;

a file system control part for acquiring access condition determined by said access condition determination part and performing file access suitable for said access condition **[see Col. 6, lines 25-40; when the memory is connected to the access device, the access device acquires and analyzes the memory card attributes, thus necessitating file system control part in the access device in order to interpret the received memory card attribute]**; and

an access control part for accessing said semiconductor memory card in response to an access request from said file system control part **[see Col. 6, lines 50-67; access device controls memory based on acquired attributes]**.

13. Regarding claim 22, Hayashi discloses an access method for accessing a semiconductor memory card in which a plurality of continuous sectors are grouped into a block as a minimum unit for data erasing and stored data is managed according to the file system comprising:

a card use condition storage step for storing information on access condition which can be used when accessing said semiconductor memory card and information on access rate desirable for said semiconductor memory card **[see Col. 6, lines 25-40; when the memory is connected to the access device, the access device acquires the memory card attributes, thus necessitating a card acquisition part in the access device]**;

a card information acquisition step for acquiring information on access on access condition as condition at the time when said access device accesses said semiconductor memory card and access performance which said semiconductor memory card realizes when said access device performs access on said access condition from said semiconductor memory card **[see Col. 6, lines 25-40; when the memory is connected to the access device, the access device acquires the memory card attributes, thus necessitating a card acquisition part in the access device]**;

an access condition determination step for determining access condition on the basis of the information acquired in said card information acquisition step and information stored in said card use condition storage step **[see Col. 6, lines 25-40; when the memory is connected to the access device, the access device acquires and analyzes the memory card attributes]**; and

a file system control step for acquiring access condition determined in said access condition determination step and accessing a file in said semiconductor memory

card so as to meet said access condition **[see Col. 6, lines 50-67; access device controls memory based on acquired attributes]**.

II. ALLOWABLE SUBJECT MATTER

Claims 10-13, 17-21 and 23-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

III. RESPONSE TO ARGUMENTS

Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection.

IV. CLOSING COMMENTS

Conclusion

(a) **Status of Claims In the Application**

(i) Claims Rejected In the Application

Per the instant office action, claims 1-27 have received a third action on the merits and are subject of a third action non-final.

(b) **Directions of Future Correspondences**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RYAN BERTRAM whose telephone number is (571)270-1377. The examiner can normally be reached on Mon-Fri 8am-4:30pm.

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on 571-272-41905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R. B./
Examiner, Art Unit 2187
/Christian P. Chace/
Supervisory Patent Examiner, Art Unit 2187